# intersil

#### **Application Note 1861**

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## ISL85415DEM01Z Wide V<sub>IN</sub> 500mA Synchronous Buck **Regulator - Short Form**

## **Description**

The ISL85415DEM01Z kit is intended for use for Point-of-Load applications sourcing from 3V to 36V. The kit is used to demonstrate the performance of the ISL85415 Wide  $\rm V_{IN}$  Low Quiescent Current High Efficiency Sync Buck Regulator with 500mA output current.

The ISL85415 is offered in a 4mmx3mm 12 Ld DFN package with 1mm maximum height. The converter occupies 1.516 cm<sup>2</sup> area.

## **Key Features**

- · Wide input voltage range 3V to 36V
- · Synchronous operation for high efficiency
- · No compensation required
- · Integrated high-side and low-side NMOS devices
- · Selectable PFM or forced PWM mode at light loads
- Internal fixed (500kHz) or adjustable switching frequency 300kHz to 2MHz
- · Continuous output current up to 500mA
- · Internal or external soft-start
- · Minimal external components required
- · Power-good and enable functions available

## **Recommended Equipment**

The following materials are recommended to perform testing:

- OV to 50V Power Supply with at least 2A source current capability
- Electronic Loads capable of sinking current up to 1.5A
- Digital Multimeters (DMMs)
- 100MHz guad-trace oscilloscope
- · Signal generator

## **Quick Setup Guide**

- 1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
- 2. Connect the bias supply to VIN, the plus terminal to VIN (P4) and the negative return to GND (P5).
- 3. Turn on the power supply.
- 4. Verify the output voltage is 3.3V for VOLT

#### Evaluating the Other Output Voltage

The ISL85415DEM01Z kit output is preset to 3.3V; however, output voltages can be adjusted from 0.6V to 15V. Please refer to the application note (AN1860 and to the ISL85415 datasheet (FN8373 for further information.

#### Frequency Control

The ISL85415 has an FS pin that controls the frequency of operation. Default switching frequency is 500kHz when FS is tied to V<sub>CC</sub>  $(R_{10} = 0)$ . By removing  $R_{10}$  the switching frequency could be changed from 300kHz ( $R_{12}$  = 340k) to 2MHz ( $R_{12}$  = 32.4k). Please refer to datasheet ISL85415 (FN8373) for calculating the value of R<sub>10</sub>. Do not leave this pin floating.

#### **Disabling/Enabling Function**

ISL85415DEM01Z board has EN pin tied to VCC via R7. This keeps the part enabled all the time. To disable the part, remove R7 and populate R8 with a  $0\Omega$  resistor.

#### **SYNC Control**

The ISL85415 evaluation board has a SYNC pin that allows external synchronization frequency to be applied. Default board configuration has  $R_6 = 200k$  to  $V_{CC}$ , which defaults to PWM operation mode and also to the pre-selected switching frequency set by R12 (see datasheet and previous section" Frequency Control" for details). If this pin is tied to GND the IC will operate in PFM mode. For PFM operation, remove R<sub>6</sub> and populate  $R_0$  with  $0\Omega$  resistor

#### Soft-Start /COMP Control

 $R_{15}$  selects between internal ( $R_{15} = 0$ ) and external soft-start.  $R_{11}$  selects between internal ( $R_{11} = 0$ ) and external compensation. Please refer to Pin Description Table (Page 3) of the ISL85415 (FN8373) datasheet.

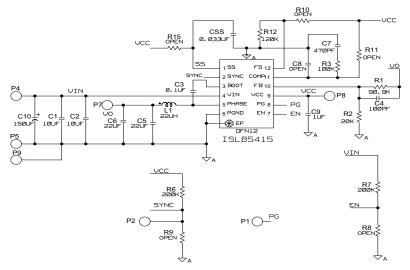
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100 V<sub>IN</sub> = 12V  $V_{IN} = 5V$ V<sub>IN</sub> = 15V 95 90 85 EFFICIENCY (%) 80 75 70 V<sub>IN</sub> = 33V V<sub>IN</sub> = 24V 65 60 55 50 L 0 0.05 0.10 0.15 0.20 0.25 0.30 0.35 0.40 0.45 0.50 OUTPUT LOAD (A) FIGURE 2. EFFICIENCY vs LOAD, PFM, V<sub>OUT</sub> = 3.3V

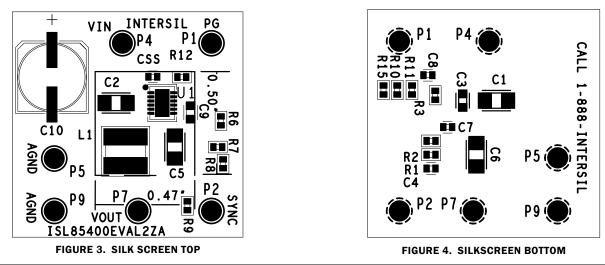
FIGURE 1. FRONT OF EVALUATION BOARD ISL85415DEM01Z

### ISL85415DEM01Z Schematic



NOTE: If the IC is used in an application where the input test leads have large parasitic inductance, the input electrolytic capacitor C10 may be added to prevent transient voltages on the input pin.

## ISL85415DEM01Z Board Layout



Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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